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MICROELECTRONICS
Digital and Analog Circuits and Systems

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MICROELECTRONICS: Digital and Analog Circuits and Systems

4567890 FGRFGR 83210

This book was set in Times Roman by Science Typographers, Inc.
The editors were Peter D. Nalle, Julienne V. Brown, and Madelaine Eichberg;
the production supervisor was Charles Hess.
New drawings were done by J & R Services, Inc.
Fairfield Graphics was printer and binder.

Library of Congress Cataloging in Publication Data

Millman, Jacob, date
Microelectronics.

Includes bibliographies and index.
1. Integrated circuits. 2. Microelectronics.
3. Electronic circuit design. 4. Digital electronics.
I. Title.
TK7874.M527 621.381'73 78-8552

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CHAPTER

FOUR

INTEGRATED CIRCUITS: FABRICATION AND CHARACTERISTICS

An integrated circuit consists of a single-crystal chip of silicon, typically 50 by 50 mils in cross section,† containing both active and passive elements and their interconnections. Such circuits are produced by the same processes used to fabricate individual transistors and diodes. These processes include epitaxial growth, masked impurity diffusion, oxide growth, and oxide etching, using photolithography for pattern definition. A method of batch processing is employed which offers excellent repeatability and is adaptable to the production of large numbers of integrated circuits at low cost. In this chapter we describe the basic processes involved in fabricating an integrated circuit.

4-1 INTEGRATED-CIRCUIT (MICROELECTRONIC) TECHNOLOGY

The fabrication of integrated circuits is based on materials, processes, and design principles which constitute a highly developed semiconductor (planar-diffusion) technology. The basic structure of an integrated circuit is shown in Fig. 4-1*b*, and consists of four distinct layers of material. The bottom layer (1) (6 mils thick) is *p*-type silicon and serves as a *substrate* or *body* upon which the integrated circuit is to be built. The second layer (2) is thin (typically 5 to 25 μm) *n*-type material which is grown as a single-crystal extension of the substrate. All active and passive components are built within the thin *n*-type layer using a series of diffusion steps. These components are transistors, diodes, capacitors, and resistors, and they are made by diffusing *p*-type and *n*-type impurities. The most complicated component fabricated is the transistor, and all other elements are constructed with one or more of the processes required to make a transistor.

† 1 mil = 0.001 in = 25.4 μm = 0.0254 mm.

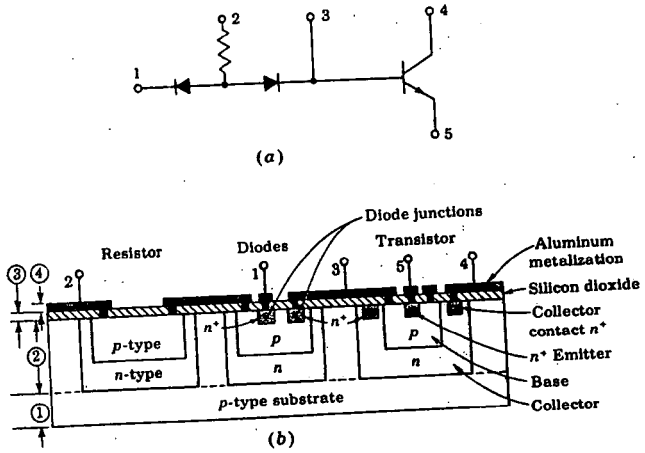


Figure 4-1 (*a*) A circuit containing a resistor, two diodes, and a transistor. (*b*) Cross-sectional view of the circuit in (*a*) when transformed into a monolithic form (not drawn to scale). The four layers are ① substrate, ② *n*-type crystal containing the integrated circuit, ③ silicon dioxide, and ④ aluminum metalization. *(After Phillips.*[2]*)*

In the fabrication of all the above elements it is necessary to distribute impurities in certain precisely defined regions within the second (*n*-type) layer. The selective diffusion of impurities is accomplished by using SiO_2 as a barrier which protects portions of the wafer against impurity penetration. Thus the third layer of material ③ is silicon dioxide, and it also provides protection of the semiconductor surface against contamination. In the regions where diffusion is to take place, the SiO_2 layer is etched away, leaving the rest of the wafer protected against diffusion. To permit selective etching, the SiO_2 layer must be subjected to a photolithographic process, described in Sec. 4-4. Finally, a fourth metallic (aluminum) layer ④ is added to supply the necessary interconnections between components.

We are now in a position to appreciate some of the significant advantages of microelectronic technology. Let us consider a 2 by 2 in wafer divided into 1,600 chips of surface area 50 by 50 mils. We demonstrate in this chapter that a reasonable area under which a component (say, a transistor) is fabricated is 50 $mils^2$. Hence each chip (each integrated circuit) contains 50 separate components, and there are $50 \times 1{,}600 = 80{,}000$ components on each wafer.

If we process 20 wafers in a batch, we can manufacture 32,000 integrated circuits simultaneously, and these contain 1,600,000 components. Some of the chips will contain faults due to imperfections in the manufacturing process, but

if the *yield* (the percentage of fault-free chips per wafer) is only 20 percent, then 6,400 good chips containing 320,000 circuit components are mass-produced in a single batch! †

The following advantages are offered by integrated-circuit technology as compared with discrete components interconnected by conventional techniques:

1. Low cost (due to the large quantities processed).
2. Small size.
3. High reliability. (All components are fabricated simultaneously, and there are no soldered joints.)
4. Improved performance. (Because of the low cost, more complex circuitry may be used to obtain better functional characteristics.)
5. Matched devices. Since all transistors are manufactured simultaneously by the same processes, the corresponding parameters of these devices as well as the temperature variation of their characteristics have essentially the same magnitudes (the parameters track well with temperature).

In the next sections we examine the processes required to fabricate an integrated circuit.

4-2 BASIC MONOLITHIC INTEGRATED CIRCUITS[1–4]

We now examine in some detail the various techniques and processes required to obtain the circuit of Fig. 4-1*a* in an integrated form, as shown in Fig. 4-1*b*. This configuration is called a monolithic integrated circuit because it is formed on a single silicon chip. The word "monolithic" is derived from the Greek *monos*, meaning "single," and *lithos*, meaning "stone." Thus a monolithic circuit is built into a single stone, or single crystal.

In this section we describe qualitatively a complete epitaxial-diffused fabrication process for integrated circuits. In subsequent sections we examine in more detail the epitaxial, photographic, and diffusion processes involved. The circuit of Fig. 4-1*a* is chosen for discussion because it contains typical components: a resistor, diodes, and a transistor. These elements (and also capacitors with small values of capacitances) are the components encountered in integrated circuits. The monolithic circuit is formed by the steps indicated in Fig. 4-2 and described below.

† The above numbers are actually quite conservative. Using the microelectronic techniques described in Chaps. 8 and 9, a component density about eight times that assumed above has been achieved on a very much larger chip. For example, an entire microprocessor (Intel 8085) containing 6,200 transistors is commercially available (in 1977) on a single chip whose dimensions are 164 by 222 mils. Hence the average area per transistor is only about 6 $mils^2$ compared with the 50 $mils^2$ used in the above calculations.

Step 1. Crystal Growth of the Substrate[4]

A tiny crystal of silicon is attached to a rod and lowered into a crucible of molten silicon to which acceptor impurities have been added. As the rod is very slowly pulled out of the melt under carefully controlled conditions, a single p-type crystal ingot of the order of 3 in (7.5 cm) in diameter and 20 in (50 cm) long is grown. The ingot is subsequently sliced into round wafers approximately 6 mils thick to form the substrate upon which all integrated components will be fabricated. One side of each wafer is lapped and polished to eliminate surface imperfections before proceeding with the next process.

Step 2. Epitaxial Growth

An n-type epitaxial layer, typically 5 to 25 μm thick, is grown into a p-type substrate which has a resistivity of approximately 10 $\Omega \cdot$ cm, corresponding to $N_A = 1.4 \times 10^{15}$ atoms/cm^3. The epitaxial process described in Sec. 4-3 indicates that the resistivity of the n-type epitaxial layer can be chosen independently of that of the substrate. Values of 0.1 to 0.5 $\Omega \cdot$ cm are chosen for the n-type layer. After polishing and cleaning, a thin layer (0.5 μm = 5,000 Å) of oxide, SiO_2, is formed over the entire wafer, as shown in Fig. 4-2*a*. The SiO_2 is grown by exposing the epitaxial layer to an oxygen or steam atmosphere while being heated to about 1000°C. Silicon dioxide has the fundamental property of preventing the diffusion of impurities through it. Use of this property is made in the following steps.

Step 3. Isolation Diffusion

In Fig. 4-2*b* the wafer is shown with the oxide removed in four different places on the surface. This removal is accomplished by means of a photolithographic etching process described in Sec. 4-4. The remaining SiO_2 serves as a mask for the diffusion of acceptor impurities (in this case, boron). The wafer is now subjected to the so-called *isolation diffusion*, which takes place at the temperature and for the time interval required for the p-type impurities to penetrate the n-type epitaxial layer and reach the p-type substrate. We thus leave the shaded n-type regions in Fig. 4-2*b*. These sections are called *isolation islands*, or *isolated regions*, because they are separated by two back-to-back p-n junctions. Their purpose is to allow electrical isolation between different circuit components. For example, it will become apparent later in this section that a different isolation region must be used for the collector of each separate transistor. The p-type substrate must always be held at a negative potential with respect to the isolation islands in order that the p-n junctions be reverse-biased. If these diodes were to become forward-biased in an operating circuit, then, of course, the isolation would be lost.

It should be noted that the concentration of acceptor atoms ($N_A \approx 5 \times$ [illegible] islands will generally be much higher

(and hence indicated as p^+) then in the p-type substrate. The reason for this higher density is to prevent the depletion region of the reverse-biased isolation-to-substrate junction from extending into p^+-type material (Sec. 2-6) and possibly connecting two isolation islands.

Parasitic Capacitance It is now important to consider that these isolation regions, or junctions, are connected by a significant barrier, or transition capacitance C_{T_2}, to the p-type substrate, which capacitance can affect the operation of the circuit. Since C_{T_2} is an undesirable by-product of the isolation process, it is called the *parasitic capacitance*.

The parasitic capacitance is the sum of two components, the capacitance C_1 from the bottom of the n-type region to the substrate (Fig. 4-2*b*) and C_2 from the sidewalls of the isolation islands to the p^+ region. The bottom component, C_1, results from an essentially step junction due to the epitaxial growth (Sec. 4-3), and hence varies inversely as the square root of the voltage V between the isolation region and the substrate (Sec. 2-6). The sidewall capacitance C_2 is associated with a diffused graded junction, and it varies as $V^{-1/3}$. For this component the junction area is equal to the perimeter of the isolation region times the thickness y of the epitaxial n-type layer. The total capacitance is of the order of a few picofarads.

Step 4. Base Diffusion

During this process a new layer of oxide is formed over the wafer, and the photolithographic process is used again to create the pattern of openings shown in Fig. 4-2*c*. The p-type impurities (boron) are diffused through these openings. In this way are formed the transistor base regions as well as resistors, the anode of diodes, and junction capacitors (if any). It is important to control the depth of this diffusion so that it is shallow and does not penetrate to the substrate. The resistivity of the base layer will generally be much higher than that of the isolation regions.

Step 5. Emitter Diffusion

A layer of oxide is again formed over the entire surface, and the masking and etching processes are used again to open windows in the p-type regions, as shown in Fig. 4-2*d*. Through these openings are diffused n-type impurities (phosphorus) for the formation of transistor emitters, the cathode regions for diodes, and junction capacitors.

Additional windows (such as W_1 and W_2 in Fig. 4-2*d*) are often made into the n regions to which a lead is to be connected, using aluminum as the ohmic contact, or interconnecting metal. During the diffusion of phosphorus a heavy concentration (called n^+) is formed at the points where contact with aluminum is to be made. Aluminum is a p-type impurity in silicon, and a large concentration of phosphorus prevents the formation of a p-n junction when the aluminum is alloyed to form an ohmic contact.[3,5]

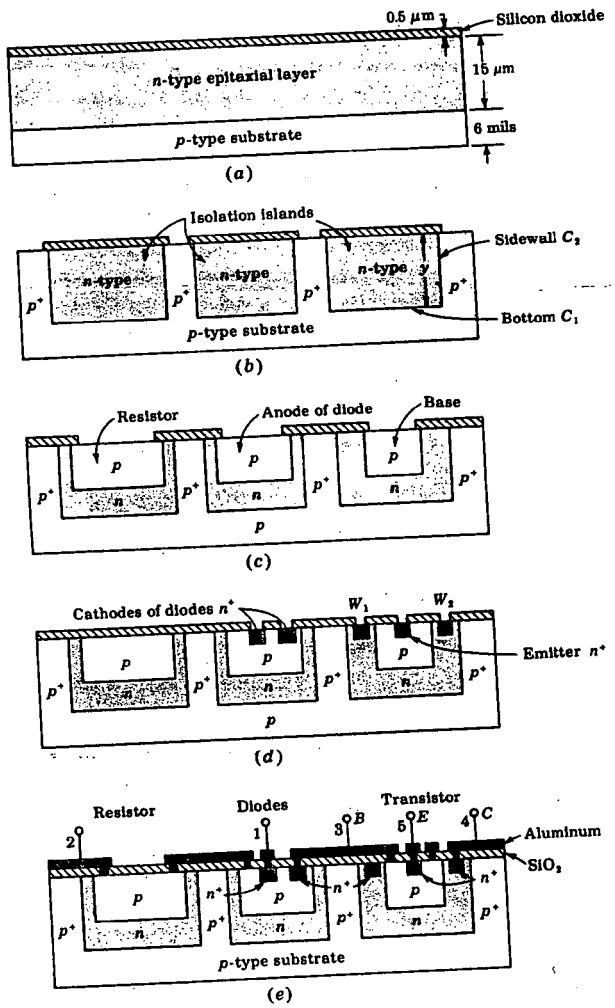


Figure 4-2 The steps involved in fabricating a monolithic circuit (not drawn to scale). (*a*) Epitaxial growth; (*b*) isolation diffusion; (*c*) base diffusion; (*d*) emitter diffusion; (*e*) aluminum metalization.

Step 6. Aluminum Metalization

All *p-n* junctions and resistors for the circuit of Fig. 4-1*a* have been formed in the preceding steps. It is now necessary to interconnect the various components of the integrated circuit as dictated by the desired circuit. To make these connections, a fourth set of windows is opened into a newly formed SiO_2 layer, as shown in Fig. 4-2*e*, at the points where contact is to be made. The interconnections are made first, using vacuum deposition of a thin even coating of aluminum over the entire wafer. The photoresist technique is now applied to etch away all undesired aluminum areas, leaving the desired pattern of interconnections shown in Fig. 4-2*e* between resistors, diodes, and transistors.

In production a large number (several hundred) of identical circuits are manufactured simultaneously on a single wafer (Fig. 4-3). After the metalization process has been completed, the wafer is scribed with a diamond-tipped tool and separated into individual chips. Each chip is then mounted on a ceramic wafer and is attached to a suitable header. The package leads are connected to the integrated circuit by stitch bonding[1] of a 1-mil aluminum or gold wire from the terminal pad on the circuit to the package lead. Most of the labor cost of an IC is in the packaging and testing (which cannot be done in a batch process).

Summary

In this section the epitaxial-diffused method of fabricating microcircuits is described. We have encountered the following processes:

1. Crystal growth of a substrate
2. Epitaxial layer growth
3. Silicon dioxide growth
4. Photoetching
5. Diffusion
6. Vacuum evaporation of aluminum

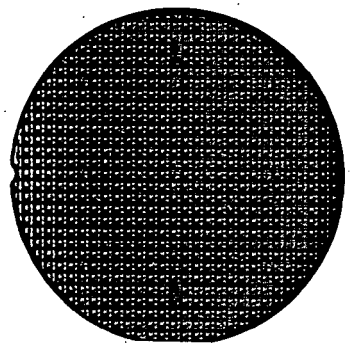
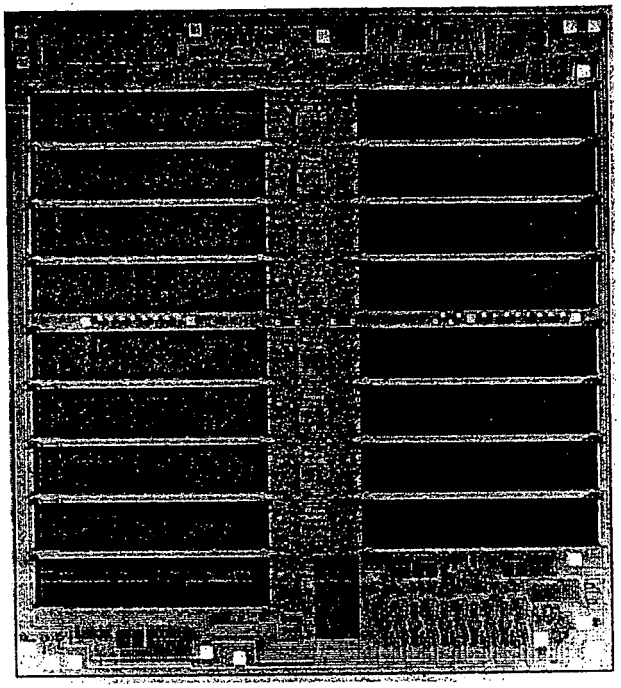


Figure 4-3 A semiconductor wafer about 2 in (5.1 cm) in diameter which includes almost 600 monolithic IC chips. *(Courtesy of IBM, Inc.)*



64 kilobits. This very large-scale integrated circuit chip employs charge-coupled device elements to provide 64,000 bits of memory. This is achieved with 16 memories of 4 k-bit each, integrated on the rather large silicon chip (0.27 cm^2). An additional 4 k-bit reference memory is used in the processing of signals, and peripheral input–output and clock generator circuits are included. This example of modern integrated circuit technology is based on principles of controlled charge transfer which cannot be understood without a firm background in semiconductor materials and devices. The purpose of this book is to provide such background, so that students may better understand and use the solid state electronic devices of the future. (Photograph courtesy of Texas Instruments, Inc.)

SOLID STATE ELECTRONIC DEVICES

second edition

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PRENTICE-HALL, INC., Englewood Cliffs, New Jersey 07632

Library of Congress Cataloging in Publication Data

STREETMAN, BEN G
Solid state electronic devices.

Bibliography: p.
Includes index.
1. Semiconductors. I. Title.
TK7871.85.S77 1979 621.3815'2 79-16994
ISBN 0-13-822171-5

Editorial/production supervision and design by Virginia Rubens
Cover design by Edsal Enterprises
Manufacturing buyer: Gordon Osbourne
Drawings by Scientific Illustrators, Champaign, Ill.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

PRENTICE-HALL INTERNATIONAL, INC., *London*
PRENTICE-HALL OF AUSTRALIA PTY. LIMITED, *Sydney*
PRENTICE-HALL OF CANADA, LTD., *Toronto*
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CONTENTS

quantity which identifies this property is the *distribution coefficient* k_d, which is the ratio of the concentration of the impurity in the solid C_S to the concentration in the liquid C_L at equilibrium:

$$k_d = \frac{C_S}{C_L} \tag{1-2}$$

The distribution coefficient is a function of the material, the impurity, the temperature of the solid–liquid interface, and the growth rate. For an impurity with a distribution coefficient of one-half, the relative concentration of the impurity in the molten liquid to that in the refeezing solid is two to one. Thus the concentration of impurities in that portion of material which solidifies first is one-half the original concentration C_0. As the zone moves along the bar, however, impurities are driven along with the molten material until the concentration in the molten zone approaches C_0/k_d. At that point as many impurities enter the zone as leave it, and Eq. (1-2) is automatically satisfied with $C_S = C_0$ and $C_L = C_0/k_d$. After the first pass, a considerable region of the ingot exists with the original impurity concentration. If another pass is made in the same direction, however, impurities are again swept with the molten zone until the condition $C_L = 2C_0$ is reached. On the second pass this point occurs farther along the bar, and the purified region is longer. If repeated passes are made, the bar can be purified over much of its length. After many passes, most of the impurities have moved to the end of the bar, which can then be cut away, leaving a highly purified crystal. Of course, if the impurity distribution coefficient k_d is smaller than the $k_d = 0.5$ case, the condition $C_L = C_0/k_d$ is reached farther along the bar, and greater purification is obtained. Many important impurities in Si and Ge have very small distribution coefficients; these impurities can be removed effectively with only a few passes of the molten zone.

The distribution coefficient, which controls the zone refining process, is also important during any growth from a melt. This can be illustrated by an example involving Czochralski growth:

EXAMPLE 1-4: A Si crystal is to be grown by the Czochralski method, and it is desired that the ingot contain 10^{16} phosphorus atoms/cm³.

(a) What concentration of phosphorus atoms should the melt contain to give this impurity concentration in the crystal during the initial growth? For P in Si, $k_d = 0.35$.

(b) If the initial load of Si in the crucible is 5 kg, how many grams of phosphorus should be added? The atomic weight of phosphorus is 31.

Solution:

(a) Assume that $C_S = k_d C_L$ throughout the growth. Thus the initial concentration of P in the melt should be

$$\frac{10^{16}}{0.35} = 2.86 \times 10^{16}\ \text{cm}^{-3}$$

(b) The P concentration is so small that the volume of melt can be calculated from the weight of Si. From Example 1-3 the density of Si is 2.33 g/cm³. In this example we will neglect the difference in density between solid and molten Si.

$$\frac{5000\ \text{g of Si}}{2.33\ \text{g/cm}^3} = 2146\ \text{cm}^3\ \text{of Si}$$

$$2.86 \times 10^{16}\ \text{cm}^{-3} \times 2146\ \text{cm}^3 = 6.14 \times 10^{19}\ \text{P atoms}$$

$$\frac{6.14 \times 10^{19}\ \text{atoms} \times 31\ \text{g/mole}}{6.02 \times 10^{23}\ \text{atoms/mole}} = 3.16 \times 10^{-3}\ \text{g of P}$$

Since the P concentration in the growing crystal is only about one-third of that in the melt, Si is used up more rapidly than P in the growth. Thus the melt becomes richer in P as the growth proceeds, and the crystal is doped more heavily in the latter stages of growth. This assumes that k_d is not varied; a more uniformly doped ingot can be grown by varying the pull rate (and therefore k_d) appropriately.

If a seed crystal is included in the starting end of the ingot of Fig. 1-14, a crystal can be grown by the *floating-zone* method. In this case the molten zone does not touch the crucible walls. As a result, such crystals have lower oxygen contamination than do Czochralski crystals, in which oxygen is dissolved by the melt in contact with the silica (SiO_2) crucible.

1.3.3 Liquid-Phase Epitaxy

It is possible to grow crystals of many semiconductors at temperatures well below their melting point. Since a mixture of the semiconductor with a second element may melt at a lower temperature than the semiconductor itself, it is often an advantage to grow the crystal from solution at the temperature of the mixture. For example, the melting point of GaAs is 1238°C, whereas a mixture of GaAs with Ga metal has a considerably lower melting point (depending on the proportions of the mixture). Thus a GaAs seed crystal can be held in a Ga + GaAs solution, which is molten at a temperature low enough that the seed itself is not melted. If the solution is cooled slowly, a single-crystal GaAs layer grows on the seed. As the GaAs leaves the solution and grows on the parent crystal, the solution becomes richer in Ga and thus has a lower melting point. Upon further cooling, more GaAs leaves the solution, and the crystal continues to grow. By this technique single crystals can be grown at temperatures low enough to eliminate many problems of impurity introduction typical of growth at the crystal melting temperature. This method is particularly useful for III–V compounds in which Ga or In serves as the column III element, since these metals form solutions at conveniently low temperatures.

The most important application of this technique is in the growth of a

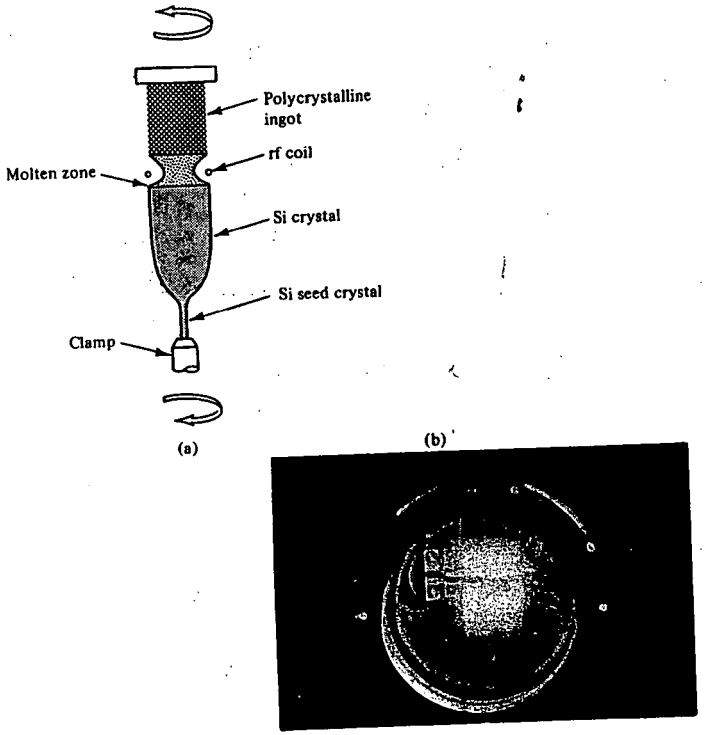


Figure 1-14. Floating-zone crystal growth: (a) schematic diagram of the growth process; (b) view through a furnace port of a Si crystal being grown by the floating-zone process. (Illustrations courtesy of Monsanto Company.)

thin crystalline layer on top of a second crystal, called the *substrate* (Fig. 1-15). The substrate crystal may be a wafer of the same material as the grown layer or of a different material with a similar lattice structure. In this process the substrate serves as the seed crystal onto which the new crystalline material grows, and also defines the shape of the growth. The growing crystal layer maintains the crystal structure and orientation of the substrate. The technique of growing an oriented single-crystal layer on a substrate is called *epitaxial growth*, or *epitaxy* (in this case, *liquid-phase epitaxy*, abbreviated *LPE*). As we shall see in the following section, other methods of epitaxial growth

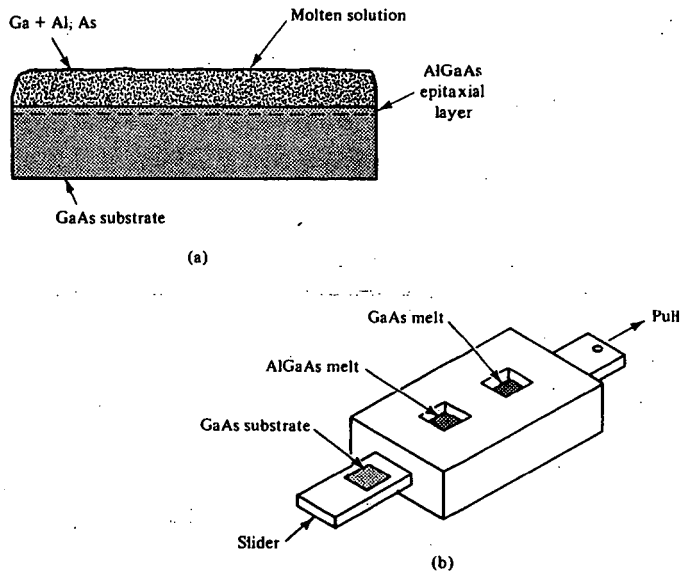


Figure 1-15. Liquid-phase epitaxial growth of AlGaAs and GaAs layers on a GaAs substrate: (a) cross section of the sample in contact with a Ga-rich melt containing Al and As; (b) carbon slider used to move the GaAs substrate between various melts. In this case, two pockets are provided, containing melts for AlGaAs and GaAs growth. The GaAs substrate on the slider is moved first into the AlGaAs growth chamber; after growth of this layer (shown in part a), the excess melt is wiped off as the slider moves the substrate to the next growth chamber.

make use of crystallization onto a substrate from a vapor (*vapor-phase epitaxy*). In LPE the solution can be placed onto the wafer in a number of ways; one of the most direct methods involves holding the wafer in a graphite slider (Fig. 1-15) and moving it into a pocket containing the melt. After growth, the epitaxial surface is wiped clean as it is moved to the next pocket, perhaps for further growth.

An obvious advantage of epitaxial growth is that pure material can be grown at temperatures well below the melting point of the semiconductor. Since the starting wafer serves mainly as a substrate, its impurity content can differ from that of the epitaxial layer grown onto it. Another important advantage of epitaxy is that a crystal of one semiconductor can be grown

on the surface of another. For example, we shall see in Chapter 10 that semiconductor diode lasers can be improved by the growth of the mixed compound AlGaAs onto a crystal of GaAs, as in Fig. 1-15.

1.3.4 Vapor-Phase Epitaxy

The advantages of low temperature and high purity which characterize LPE growth can also be achieved by crystallization from the vapor phase. Crystalline layers can be grown onto a seed or substrate from a chemical vapor of the semiconductor material or from mixtures of chemical vapors containing the semiconductor. *Vapor-phase epitaxy (VPE)* is a particularly important source of semiconductor material for use in devices. Some compounds such as GaAs can be grown with better purity and crystal perfection by vapor epitaxy than by other methods. Furthermore, these techniques offer great flexibility in the actual fabrication of devices. When an epitaxial layer is grown on a substrate, it is relatively simple to obtain a sharp demarcation between the type of impurity doping in the substrate and in the grown layer. The advantages of this freedom to vary the impurity will be discussed in subsequent chapters. We point out here, however, that bipolar Si integrated-circuit devices (Chapter 9) are usually built in layers grown by vapor epitaxy on Si wafers.

Epitaxial layers are generally grown on Si substrates by the controlled deposition of Si atoms onto the surface from a chemical vapor containing Si. In one method, a gas of silicon tetrachloride reacts with hydrogen gas to give Si and anhydrous HCl:

$$SiCl_4 + 2H_2 \longrightarrow Si + 4HCl \qquad (1\text{-}3)$$

If this reaction occurs at the surface of a heated crystal, the Si atoms released in the reaction can be deposited as an epitaxial layer. The HCl remains gaseous at the reaction temperature and does not disturb the growing crystal.

The apparatus necessary for this vapor epitaxy technique is shown schematically in Fig. 1-16. The Si slice is heated in a silica tube into which the gases can be introduced. Since the chemical reactions take place in this chamber, it is called a *reaction chamber* or, more simply, a *reactor*. Hydrogen gas is passed through a heated chamber in which $SiCl_4$ is evaporated; then the two gases are introduced into the reactor over the substrate crystal, along with other gases containing the desired doping impurities. The Si slice is placed on a graphite susceptor or some other material which can be heated to the reaction temperature with an rf heating coil. This method can be adapted to grow epitaxial layers of closely controlled impurity concentration on many Si slices simultaneously.

The reaction temperature for the hydrogen reduction of $SiCl_4$ is approximately 1250°C. Other reactions may be employed at somewhat lower temperatures, including the pyrolysis of silane (SiH_4) at 1000°C. Pyrolysis involves the breaking up of the silane at the reaction temperature:

$$SiH_4 \longrightarrow Si + 2H_2 \qquad (1\text{-}4)$$

There are several advantages of this technique, including the fact that the lower reaction temperature reduces migration of impurities from the substrate to the growing epitaxial layer.

In some applications it is useful to grow thin Si layers on insulating substrates. For example, vapor-phase epitaxial techniques can be used to grow $\sim 1\mu$m Si films on sapphire. This application of VPE is discussed in Section 9.3.3.

Vapor-phase epitaxial growth is also important in the III–V compounds, such as GaAs, GaP, and the ternary alloy GaAsP. The latter material is widely used in the fabrication of light-emitting diodes (LEDs). Figure 1-17 illustrates schematically a vapor-phase reactor for the growth of these materials. Substrates are held at about 800°C on a rotating wafer holder while phosphine, arsine, and gallium chloride gases are mixed and passed over the samples. The GaCl is obtained by reacting anhydrous HCl with molten Ga within the reactor. This particular VPE system is well suited for commercial production of epitaxial crystals, handling up to 50 in.^{2} of substrate

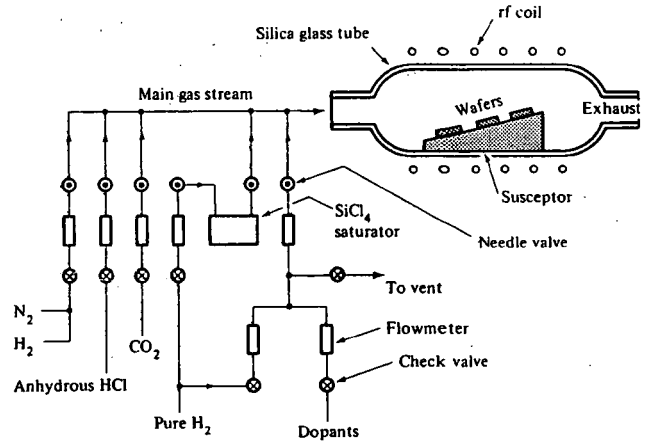


Figure 1-16. Typical deposition system for Si vapor epitaxy using a $SiCl_4$ source. (After B. M. Berry, "Epitaxy," in *Fundamentals of Silicon Integrated Device Technology*, vol. I, ed. R. M. Burger and R. P. Donovan. Englewood Cliffs, N.J.: Prentice-Hall, Inc., © 1967, p. 365.)

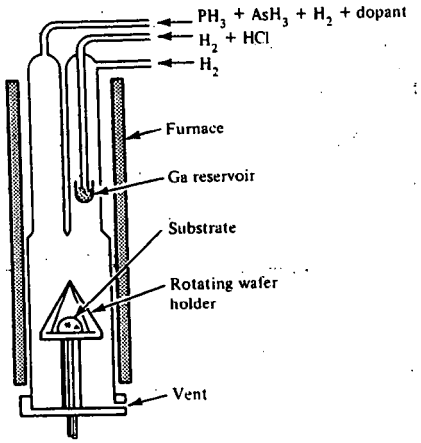


Figure 1-17. Schematic diagram of a vapor-phase epitaxial (VPE) reactor used to grow GaAs, GaP, and the mixed-compound GaAsP. (Illustration courtesy of Monsanto Company.)

wafers per growth run. Variation of the crystal composition for GaAsP can be controlled by altering the mixture of arsine and phosphine gases.

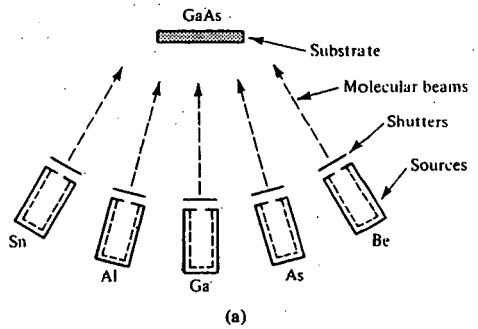
Another useful method for growing compound semiconductors is called *metal organic* (or *organometallic*) growth. For example, trimethylgallium can be reacted with arsine to form GaAs and methane:

$$(CH_3)_3Ga + AsH_3 \longrightarrow GaAs + 3CH_4 \qquad (1\text{-}5)$$

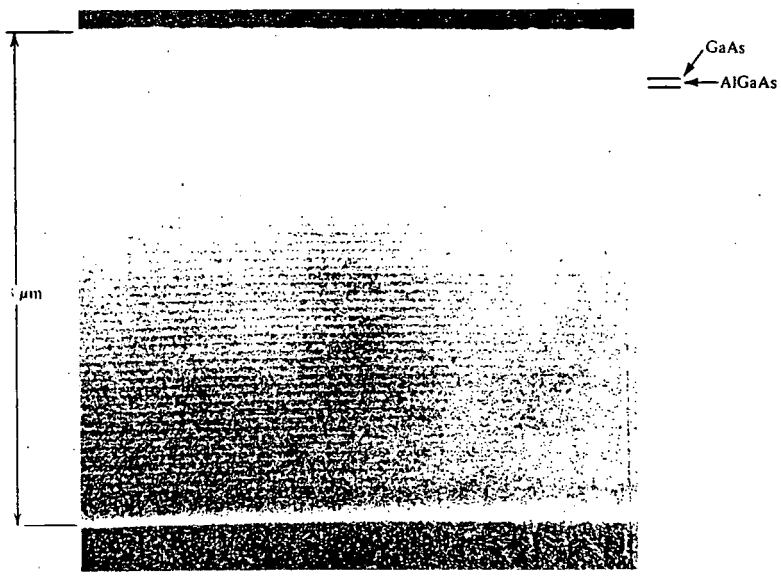
This reaction takes place at about 700°C, and epitaxial growth of high-quality GaAs layers can be obtained. Other compound semiconductors can also be grown by this method. For example, trimethylaluminum can be added to the gas mixture to grow AlGaAs. This growth method has been used in the fabrication of a variety of devices, including solar cells and lasers. The convenient variability of the gas mixture allows the growth of multiple thin layers similar to those discussed below for molecular beam epitaxy.

1.3.5 Molecular Beam Epitaxy

One of the most versatile techniques for growing epitaxial layers is called *molecular beam epitaxy* (*MBE*). In this method the substrate is held in a high vacuum while molecular or atomic beams of the constituents impinge upon its surface (Fig. 1-18). For example, in the growth of AlGaAs layers on GaAs substrates, the Al, Ga, and As components, along with dopants, are



(a)



(b)

Figure 1-18. Crystal growth by molecular beam epitaxy (MBE): (a) evaporation cells inside a high-vacuum chamber directing beams of Al, Ga, As, and dopants onto a GaAs substrate; (b) scanning electron micrograph of the cross section of an MBE-grown crystal having 100 alternating layers of GaAs (80 Å per layer) and AlGaAs (400 Å). (Photograph courtesy of Bell Laboratories.)